THE DINI GROUP

DVI DAUGHTER CARD

User Guide
DNDVI_DC

LOGIC EMULATION SOURCE

DNDVI_DC User Manual Version 1.1

© The Dini Group

1010 Pearl Street • Suite 6
La Jolla, CA92037
Phone 858.454.3419 • Fax 858.454.1279
support@dinigroup.com
www.dinigroup.com

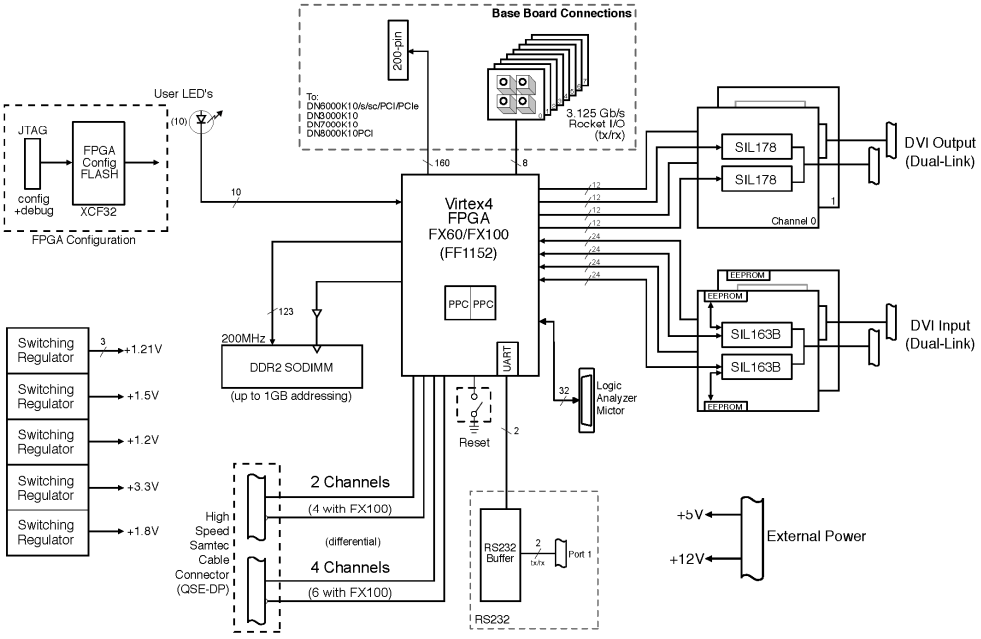
Last Modified: 8/3/2007 11:12:51
Last saved by jthurkettle

Chapter

0

Welcome to DNDVI_DC Daughter Card

Congratulations on your purchase of the DNDVI_DC Daughter Card!



Chapter 1

1 Quick Start Guide

The Dini Group DNDVI_DC is the user-friendliest board available with a Virtex 4 FPGA and two DVI interface

1.1 What's provided

First, let's examine the contents of your DNDVI_DC kit. It should contain:

- DNDVI_DC board
- RS 232 IDC header cable to female DB9
- CD ROM containing:
  - Virtex 4 Reference Design
  - User manual PDF
  - Board Schematic PDF
  - DNDVI_DC firmware

The Dini Group can optionally provide the following accessories:

- Memory modules for use in the DNDVI_DC DDR2 SODIMM socket

  - QDRII SRAM 64x1Mb, 300Mhz
  - Flash memory 32x4Mb, 2x4Mb serial flash
  - Reduced Latency DRAM (RLDRAM) 64x8Mb, 300Mhz
  - Standard SRAM, 64x2M (Select ZBT/sync-burst, Pipelined/Flow through)
  - Test connection module (with two Mictor38)

You may also want to obtain from a third party vendor:

- Xilinx Parallel Cable IV or Xilinx Platform Cable USB
- 200-pin DDR2 SODIMM
- Synplicity Identify, or Xilinx Chipscope for embedded logic analyzer functionality.
- LCD monitor with DVI input [Any DVI 1.0 compliant monitor should suffice].
- Video card with DVI output.
- Video camera with DVI output.

1.2 Precaution

The DNDVI_DC is sensitive to static electricity, so treat the PCB accordingly. The target markets for this product are engineers that are familiar with FPGAs and circuit boards. However, if needed, the following web page has an excellent tutorial on the "Fundamentals of ESD" for those of you who are new to ESD sensitive products:

http://www.esda.org/basics/part1.cfm

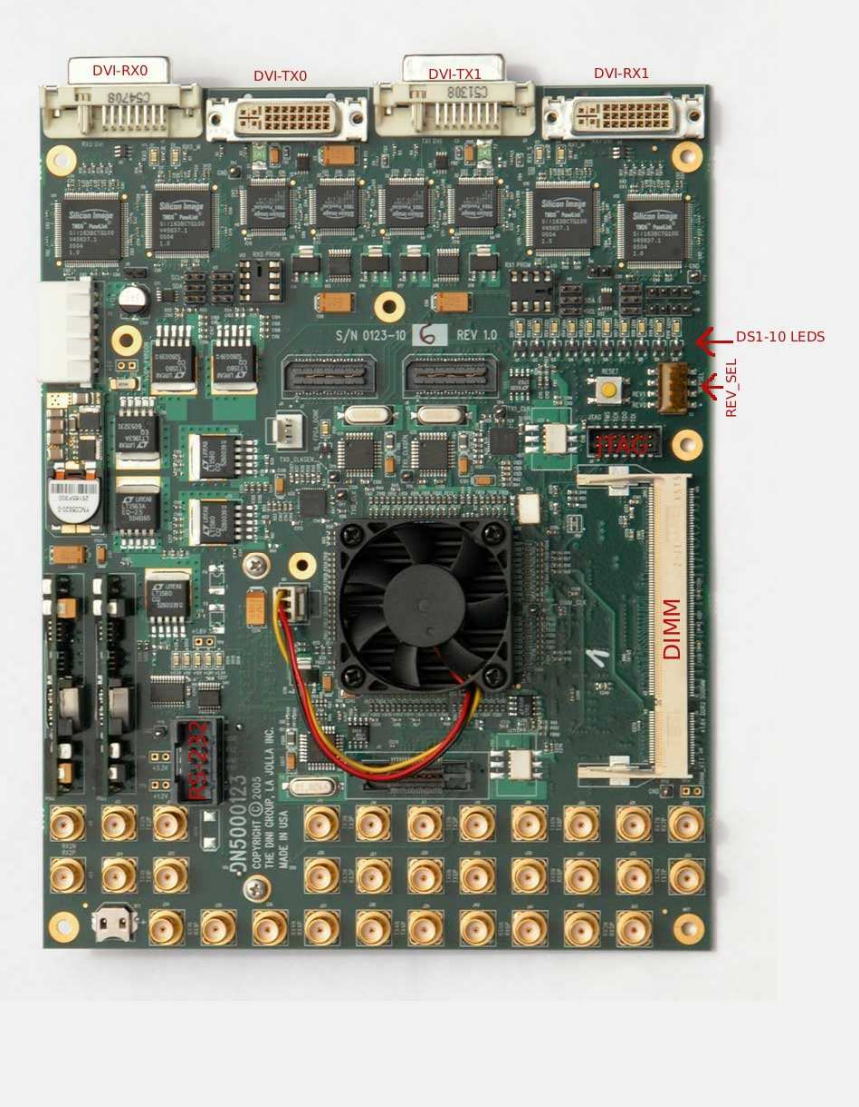
There are four ground test points on the DNDVI_DC.

The DNDVI_DC has been factory tested and pre-programmed to ensure correct operation. You do not need to alter any jumpers or program anything to see the board work. A reference design is included on the provided CD.

The 200-pin connector is not 5V tolerant. According to the Virtex 4 datasheets, the maximum applied voltage to these signals is VCCO + 0.5V (3.0V while powered on). These connections are not buffered, and the Virtex 4 part is sensitive to ESD. Take care when handling the board to avoid touching the daughter card connectors.

1.3 Power-On Instructions

The image below represents your DNDVI_DC. You will need to know the location of the following parts referenced in this chapter.



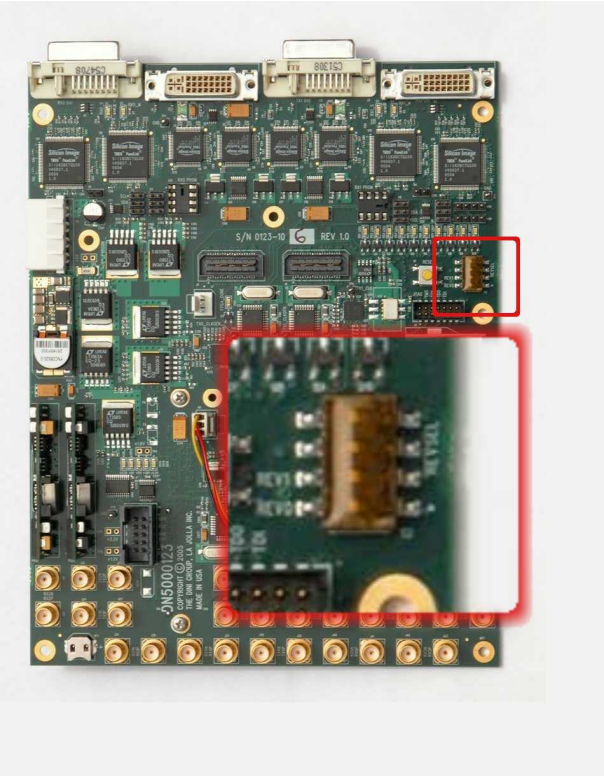
To begin working with the DNDVI_DC, follow the steps below :

1.4 Verify Switch Settings

The DNDVI_DC uses a DIP switch to program the FPGA configuration circuitry. The function of these DIP switches is listed in Table 2. Verify that the switch settings on your board match the default settings.

Table 1 - Switch Description

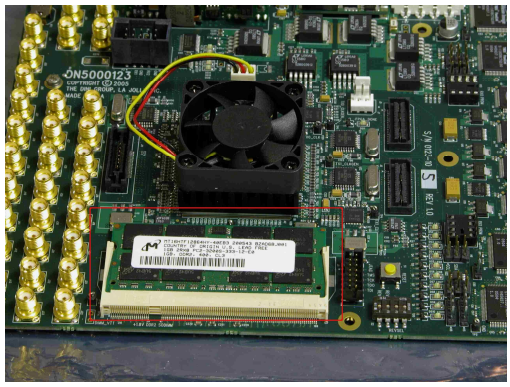
Switch	Default Position	Signal Name	On setting	Off setting
S1-1	Off	CFG_REV0	When CFG_REVSEL is ON - CFG_REV0 and CFG_REV1 are used to select the design revision to be enabled, overriding the internal programmable revision selection control bits.	
S1-2	Off	CFG_REV1		
S1-3	Off	CFG_REVSEL		
S1-4	Off	DIPSW4	Configurable	Configurable



1.5 Memory and heat sinks

There should be an active heat sink installed on the FPGA on the DNDVI_DC. Virtex 4 FPGAs are capable of dissipating 15W or more, so you should always run the board with the heat sink installed.

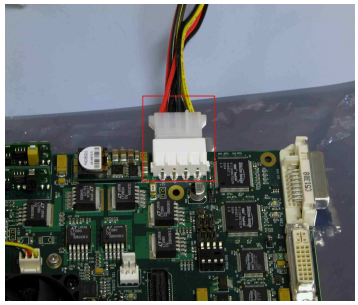
The DNDVI_DC comes packaged without memory installed. If you want the Dini Group reference design to test your memory module, you can install it now in the 1.8V DDR2 DIMM socket.



The socket DDR2_SODIMM can accept any capacity DDR2 SODIMM. Note that DDR1 modules will not work in these slots since they are supplied with 1.8V power and DDR1 requires 2.5V power (and a completely different pin-out). [Note that the Dini Group has a DDR2 module that provides a DDR1 socket, even so, changing all the voltages would still be required.]

1.6 Power Up Procedure

1. Plug the four pin hard drive power connector from the power supply into P2. Make sure your work area is clear and there are no metal wrenches under the board. Turn on the power supply.



When the DNDVI_DC powers on, it automatically loads Xilinx FPGA design bit file stored in the PROM (if the load FPGA option was selected during PROM programming).

To load a different Xilinx bit program file into the DNDVI_DC follow the steps outlined in section 2.4.

1.7 Loading FPGA configuration once

The DNDVI_DC reads FPGA configuration data from the JTAG chain. To program the FPGA on the DNDVI_DC, FPGA design file (with a .bit file extension) are uploaded through the JTAG chain. This can be accomplished using the Xilinx ISE iMPACT tool.

Step by step instructions for loading bit file into the FPGA via iMPACT.

1. Attach the Xilinx JTAG cable to J8 on the DNDVI_DC

2. Start iMPACT.

3. Create a new project in iMPACT [file -> new -> create new project]
4. Choose "Configure devices using Boundary-Scan (JTAG)" as the project action.
5. Bypass the first "Assign New Configuration File" pop-up menu.
6. Select the FPGA design bit file in the second "Assign New Configuration File" pop-up menu.
7. Right click on the FPGA in the JTAG chain display select program and then OK at the "Programming Properties" menu.

1.8 Loading FPGA bitfile into the PROM

There is an XCF32P Xilinx FLASH-PROM on the board to allow the FPGA to automatically be programmed when the board is powered on. To use this feature, the ISE tools must be version 7.1sp3 or newer.

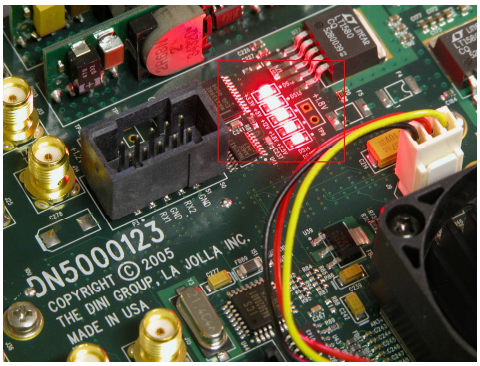
1. Attach a Xilinx JTAG cable to J8 on the DNDVI_DC.
2. Start iMPACT.
3. Create a new project in iMPACT.
4. Choose "Prepare a PROM File" as the project action.
5. Target: "Xilinx PROM", "MCS" file format, and give it a filename.
6. Select an "xcf32p" as the PROM Device, and add it to the list.
7. When it brings up the GUI, and asks for a ".bit" file, give it your ".bit" file generated by the ISE tools. Don't add a second ".bit" file, because there is only 1 FPGA on the board.
8. Now generate the ".mcs" output file by double clicking on "Generate File". Go check to make sure that the ".mcs" file was created.
9. To program that ".mcs" file into the Prom:
    a. Switch iMPACT to boundary scan mode.
    b. Initialize the JTAG chain. It should find the "xcf32p" and the "xc4vfx60/100" devices.
    c. Assign the ".mcs" file as the programming file for the "xcf32p".
    d. "Bypass" the programming file for the "xc4vfx60/100".
    e. Double click "Program" while the "xcf32p" is selected. Make sure to select "Verify", "Erase Before Programming", and "Load FPGA" from the options given in the programming window. Hit "OK" and wait for about 2 minutes until the programming has completed.

10. Now when the board is power-cycled, it will automatically have the ".mcs" file loaded into the FPGA.

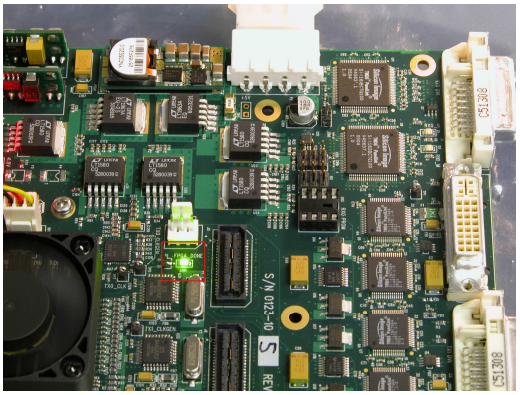
1.9 Check LED status lights

The DNDVI_DC has many status LEDs to help the user confirm the status of the configuration process.

1. Check the power voltage indication LEDs to confirm that all voltage rails of the DNDVI_DC are present. The LEDs indicate the presence of 12V, 5V, 3.3V, 2.5V, and 1.8V



2. Check the Configuration status LED. When the FPGA has been successfully configured the FPGA_DONE LED will illuminate.



You should also verify the fan mounted above the Virtex 4 FPGA is spinning.

1.10 Finished Quick Start

At this point either a reference design is loaded or a user supplied design is loaded in the DN_DVI board. If you wish to verify the reference design move on to chapter 2.

Chapter 2

2 Testing the Reference design using the Included software

To test the reference design on the daughter card, the DNDVI_DC provides tests for the following options out of the box.

- DVI RX0, RX1, TX0, TX1
- 200-pin SODIMM socket
- RS232 Loopback
- Rocket IO

The 4 DVI connectors allow single-link and dual-link digital video to be received and transmitted.

The RS232 interface allows low-speed data transfers to and from the User design.

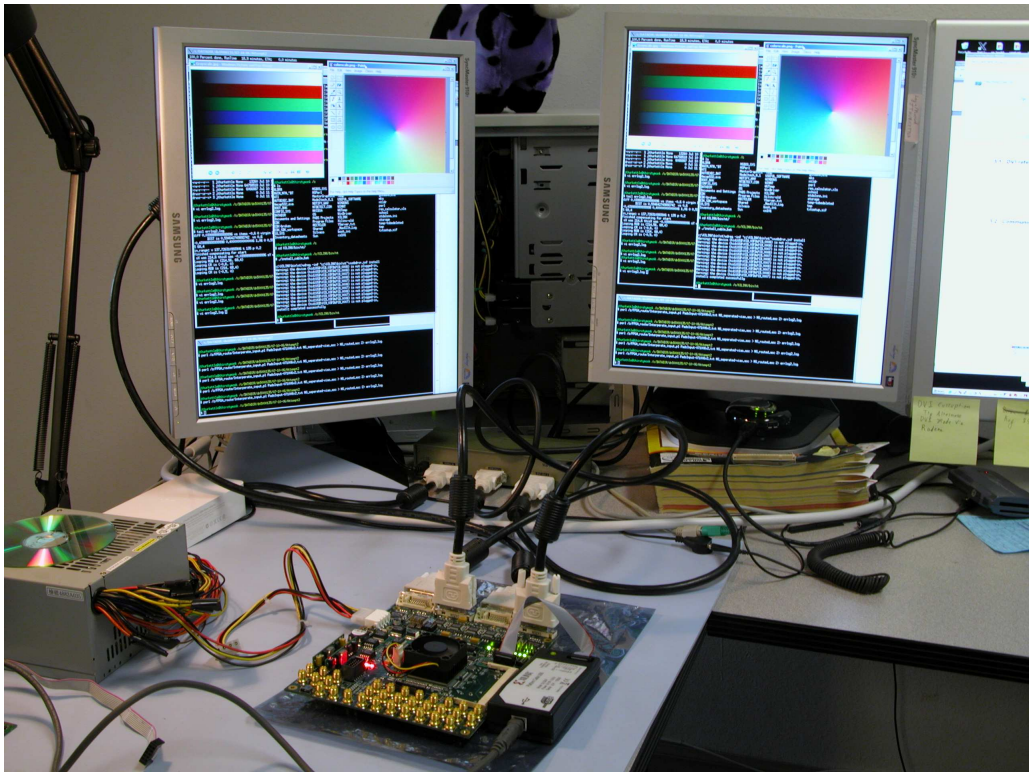
A DDR2 SDRAM SODIMM can be installed in the 200-pin SODIMM socket, or one of our other cards (SSRAM, FLASH, Mictor, …) can be installed instead.

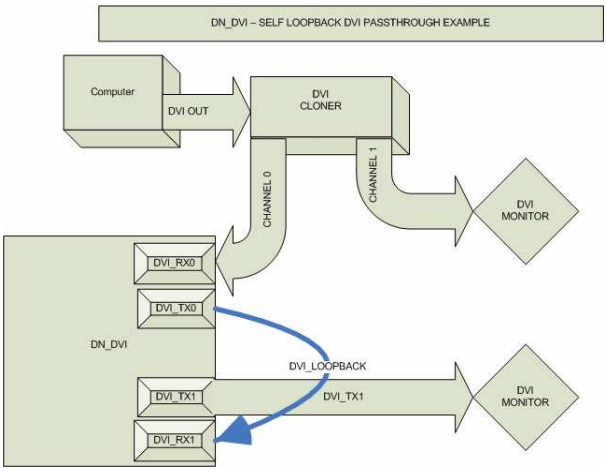
The 200-pin header can be used to connect the DNDVI_DC to many of the DiniGroup FPGA emulation boards (check http://www.dinigroup.com for the compatibility list).

This section will get you started and show you how to operate the provided software.

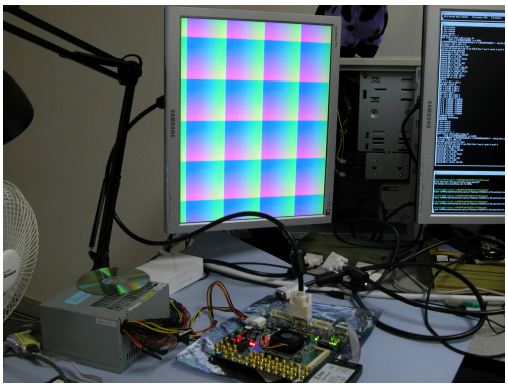
2.1 DVI reference design

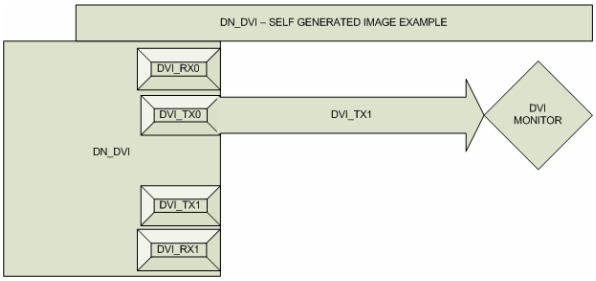
The FPGA is initially programmed with a reference design that will receive DVI video on RX0, and send it back out on TX0. (The RST switch may need to be applied after changing input frequencies). The same is true for RX1 and TX1.



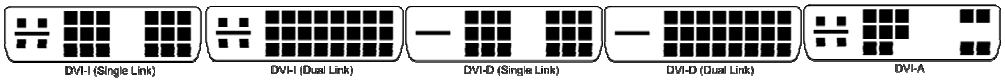


There is also sample code that can be un-commented in the reference design that will generate a simple video output pattern (without requiring a DVI input cable connected to RX0).





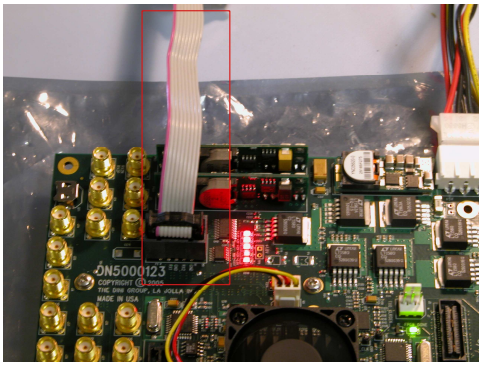
NOTE: If you are using a dual link signaling you **MUST** use dual link DVI cables. Dual link DVI cables can be identified by the pin out on the connector.



2.2 Communicating to the User Design over the Serial Port

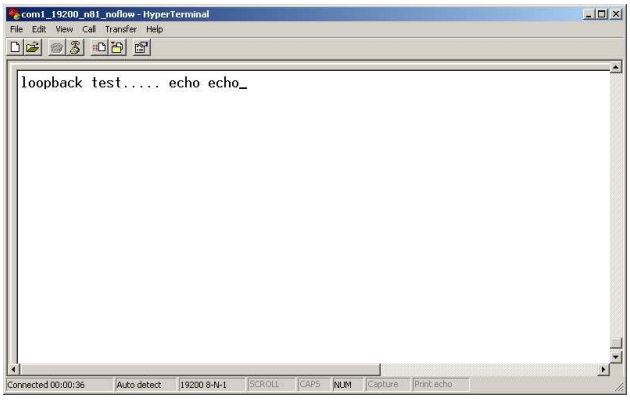
You may want to communicate with your design over the user serial port (P3).

Connect a RS232 cable to P3, the FPGA RS232.



The reference design is programmed to digitally loop back the input to the output. No hardware flow control is supported. If on the terminal you see a local echo, then the

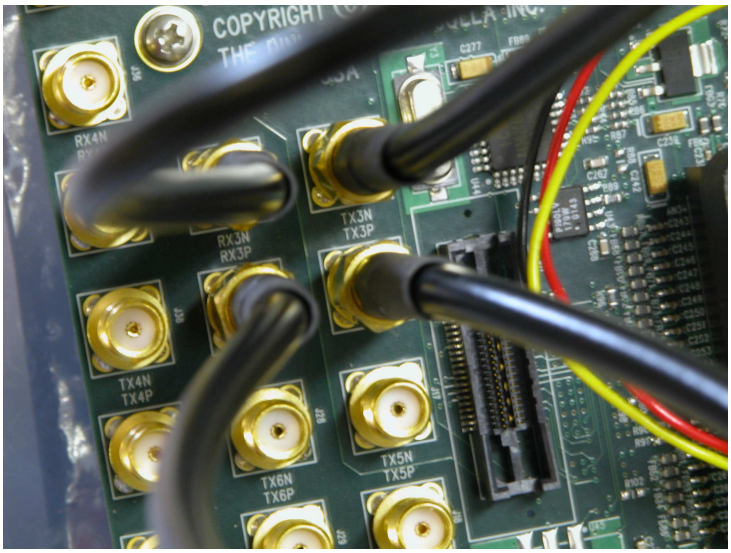
reference design was able to capture the RS232 signal and generate an RS232 signal that your computer could capture.



2.3 DDR2 SODIMM TEST

The provided test design automatically runs a DDR2 memory test with status indicated by the LEDs. After reset LED 5 will go high for approximately 20 seconds followed by LED indicators of the memory test. LED10-9 indicate test stage. 00 indicates initial stage, 01 indicates write read test, 10 indicates read back test, 11 indicates successful completion of tests. If an error occurs the LEDS will indicate which test failed and indicate the LSB of error in the memory.

2.4 RocketIO TEST



On the CD accompanying the DNDVI board in the bit file directory one can find the RocketIO MCS file. Load the MCS file into the PROM following the steps outlined in section 2.5. Connect SMA cables in loop back configuration on all eight of the RocketIO pairs. [That is to say connect TXP to RXP and TXN to RXN]. Reset or power on the board after all the connections have been made. If test passes all 10 LEDS should flash on and off. The image above shows the loopback configuration for pair 3.

The following is an explicit list of pair matching.

[J12-J13], [J23-J14], [J24-J34], [J25-J35], [J36-J38], [J37-J39], [J26-J15], [J27-J16], [J28-J40], [J29-J41], [J17-J42], [J18-J43], [J30-J19], [J31-J20], [J32-J21], [J33-J22]

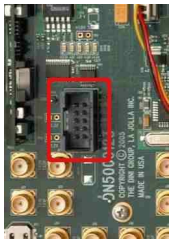
Chapter 3

3 DNDVI_DC Hardware

3.1 ERRATA

Please note – On the Revision 1.0 boards a jumper wire has been added to the bottom of the board between R244 and the non-power side of R325. This is not reflected in the schematic.

3.2 Multiplexed Serial Port



The DNDVI_DC has one serial port (P3) for user use. No configuration is required to enable the first serial port. This can be extended to two serial ports by use of a breakout serial cable. LED5 and LED6 are tied to the second serial ports TX and RX respectively.

Serial port 1 uses pins 2 and 3. Serial port 2 uses pins 6 and 7 of port P3.

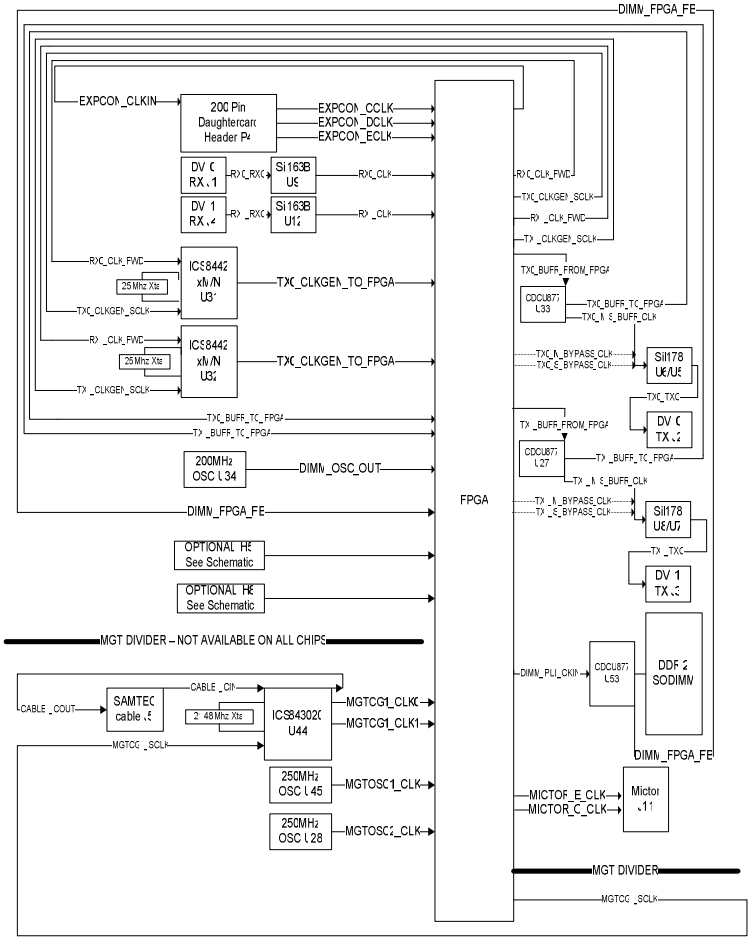
To enable the second RS232 Port: Add the following 0 Ohm resistors. R350, R352, R362, R360. This will enable the second serial port on pins 6 and 7 on P3. For more details see page 07 in the Schematic. "P07: MISC. PERIPHERALS".

Chapter

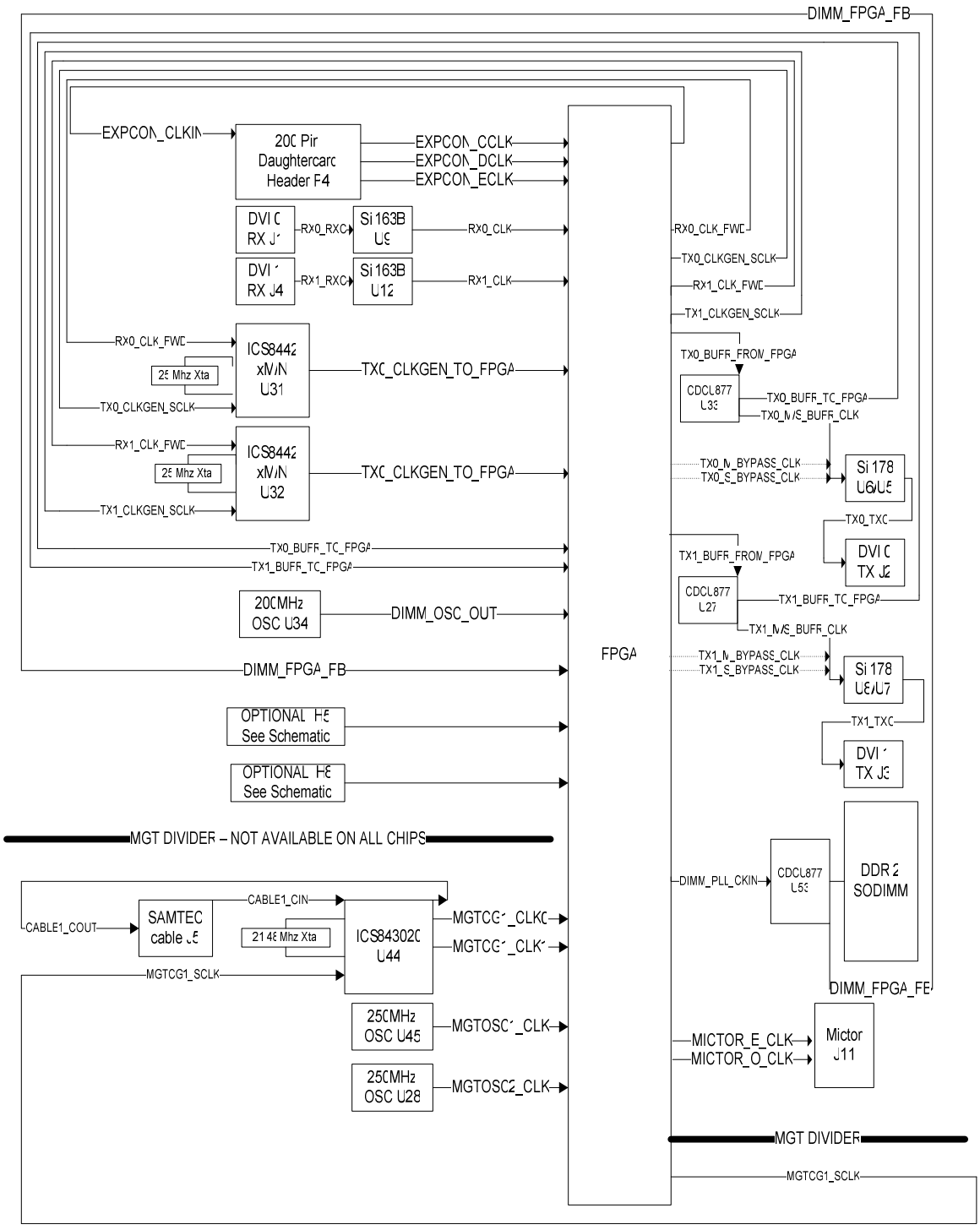
4

4 Clocking Overview

This chapter discusses the various clocks available on the DNDVI_DC and any user settable options available.



4.1 Block Diagram of the DNDVI_DC clocks:



4.2 List of Input Clocks

When shipped the DNDVI board has several clock sources available.

DIFFERENTIAL:

- 200 Mhz Oscillator [U34] : H17/J17
- 250 Mhz Oscillator [U45] : M34/N34 [for MGT use only]
- 250 Mhz Oscillator [U28] : J1/K1 [for MGT use only]
- ICS8442 Clock Generator [U31]: J16/J15
- ICS8442 Clock Generator [U32]: J14/K14
- ICS843020 Clock Generator [U44]: [AP29/AP28], [AP3/AP4] : [for MGT use only]
- Note: Pins 2/3 on H5 can be configured as an input clock at the expense of two LEDs - See Schematic page P09_CLOCKS for details: H19/H18.
- Note: Pins 2/3 on H8 can be configured as an input clock at the expense of two LEDs - See Schematic page P09_CLOCKS for details: AF18/AG18.

DIFFERENTIAL FEEDBACK CLOCKS:

- TX0 PLL CDCU877 [U33]: K18/K17
- TX1 PLL CDCU877 [U27]: K19/J19
- DDR PLL CDCU877 [U53]: L15/L14

SINGLE ENDED CLOCKS:

- RX0 [U9]: AD21
- RX1 [U12]: AE18
- EXPCON_CCLK [P4] : AF16
- EXPCON_DCLK [P4] : AG17
- EXPCON_ECLK [P4]: AE21

4.3 List of Output Clocks

SINGLE ENDED CLOCKS:

- EXPCON_CLKIN [P4]: AF20
- GP_I2C_SCL : AE17 : Note that this is the general I2C clock for the board and attaches to both the FPGA temperature sensor and the DDR2 connector.
- RX0_CLK_FWD [U31]: U7 - Note: By default this clock is ignored on the ICS8442, see schematic for details.
- RX1_CLK_FWD [U32]: U6 - Note: By default this clock is ignored on the ICS8442, see schematic for details.
- RX0_I2C_SCL [U21]: AH9
- RX1_I2C_SCL [U22]: V3
- TX0_I2C_SCL [U6/U3]: AF13 – Note: This attaches to both the SIL178 and J2 output.
- TX1_I2C_SCL [U4/U8]: AM10 -- Note: This attaches to both the SIL178 and J3 output.
- TX0_CLKGEN_SCLK [U31]: L31
- TX1_CLKGEN_SCLK [U32]: L30
- MGTCG1_SCLK [U44]: J32
- TX0_M_BYPASS_CLK : AB5 – Note: Ignored by default, see schematic for details.
- TX0_S_BYPASS_CLK : AD5 – Note: Ignored by default, see schematic for details.
- TX1_M_BYPASS_CLK : AG8 – Note: Ignored by default, see schematic for details.
- TX1_S_BYPASS_CLK : AG7 – Note: Ignored by default, see schematic for details.
- MICTOR_E_CLK [J11] : F29

- MICTOR_O_CLK[J11] : E29

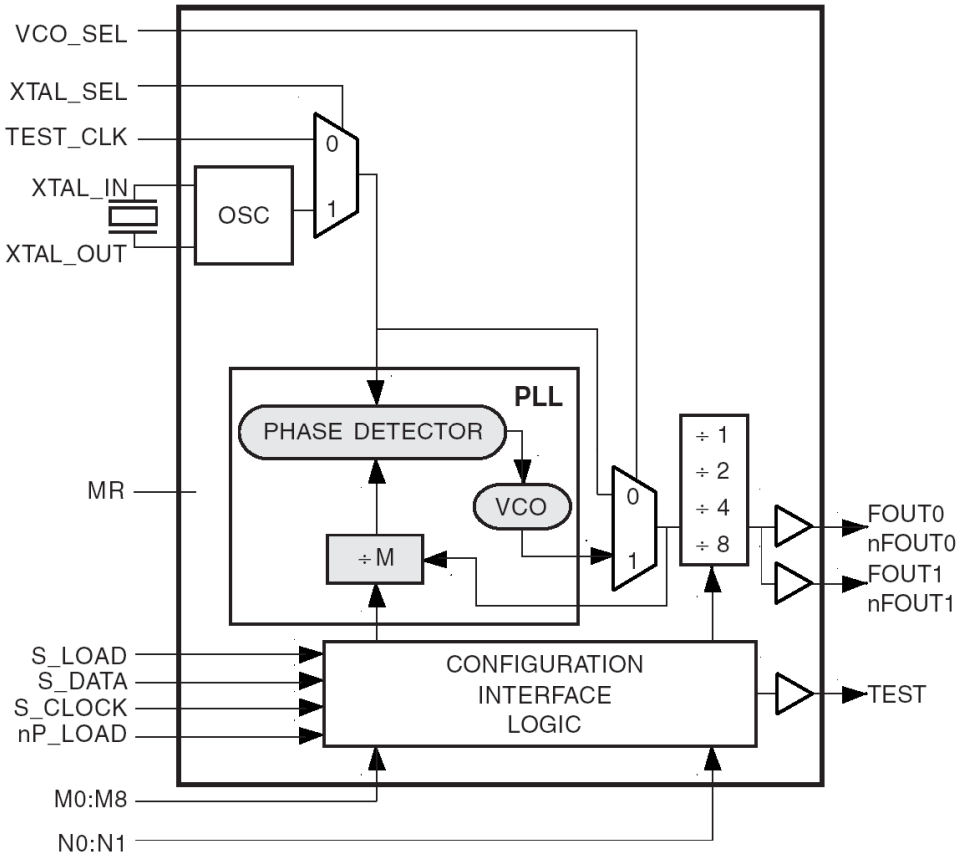
DIFFERENTIAL CLOCKS:

- DIMM_PLL_CKIN [U53] : AD7/AD6
- TX0_BUFR_FROM_FPGA [U33] : AB3/AA3
- TX1_BUFR_FROM_FPGA [U27] : AM3/AL3

4.4 Configuring the ICS8442s [U31, U32]

Note that the ICS8442 reference manual should be considered the authority concerning any of the ICS8442s. The manual is available on the DNDVI CD as ICS8442.pdf and also from the ICS website.

http://www.icst.com/datasheets/ics8442.pdf

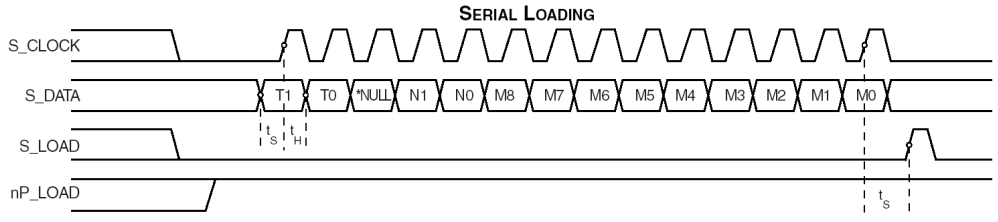


Note a ICS8442 simulation only Verilog model is included in the reference design.

The ICS8442 has two modes of operation: Input from TEST_CLK or input from XTAL_IN/OUT depending on the setting of XTAL_SEL. By default XTAL_SEL is set to 1 [XTAL_IN/OUT] to switch the input into the 8442s see the Schematic, one will need to move a configurable resistor going into XTAL_SEL.

The FOUT frequency is governed by **FOUT = F_IN * M/2^N;** Where M is an integer and N is a power of two. FOUT is a LVDS differential signal and must be treated as such when being incorporated into the Verilog/VHDL design.

Only serial configuration is supported on the DN_DVI board which means the 8442 needs to be configured each time the board is reset.



In addition to the above discussed N and M inputs T configures the TEST output a pattern of {1,1} will set TEST to FOUT.

Note that the SDATA and SLOAD are the same for all the ICS8442s on the DNDVI board and that each ICS8442 can be programmed separately by control of the individual S_CLOCK signals. Please see the schematic for specific ICS8442s. The maximum frequency allowable for S_CLOCK is 50MHZ, LVCMOS.

When editing the constraints file for a design make sure the ICS8442 inputs are set to LVDSEXT_25; And that DIFF_TERM is used on the input buffer. [See note on Schematic P09_CLOCKS].

Example FOUT Verilog/VHDL/UCF settings:

UCF: NET "..FOUT.." LOC = … | IOSTANDARD = LVDSEXT_25;

Verilog: IBUFGDS

Verilog: #(.DIFF_TERM("TRUE"))

Verilog: IGDS_FOUT

Verilog: (.I(FOUT_P), .IB(FOUT_N), .O(FOUT_IGDS));

VHDL: IGDS_FOUT: IBUFGDS

VHDL: generic map (

VHDL: DIFF_TERM => "TRUE")

VHDL: port map (

VHDL: I => FOUT_P , IB => FOUT_N ,

VHDL: O => FOUT_IGDS) ;

4.5 Configuring the CDCU877 [U27, U33, U53]

Note that the CDCU877 reference manual should be considered the authority concerning any of the CDCU877s. The manual is available on the DNDVI CD as CDCU877.pdf and also from the Texas Instrument website.

http://focus.ti.com/docs/prod/folders/print/cdcu877.html

http://www-s.ti.com/sc/ds/cdcu877.pdf

The CDCU877 can either be set in BYPASS mode where the input clock is sent directly to the outputs or in PLL mode. PLL mode is set by holding AVDD to VDD [+1.8V]. BYPASS mode is set by grounding AVDD. Please see the schematic for details about which components to add and remove [Removing a Ferrite bead and adding 0 Ohm resistors].

When editing the constraints file for a design make sure the CDCU877 inputs are set to LVDSEXT_25; And that DIFF_TERM is used on the input buffer. [See note on Schematic P09_CLOCKS].

Example FOUT Verilog/VHDL/UCF settings:

UCF: NET "..FOUT.." LOC = … | IOSTANDARD = LVDSEXT_25;

Verilog: IBUFGDS

Verilog: #(.DIFF_TERM("TRUE"))

Verilog: IGDS_FOUT

Verilog: (.I(FOUT_P), .IB(FOUT_N), .O(FOUT_IGDS));

VHDL: IGDS_FOUT: IBUFGDS

VHDL: generic map (

VHDL: DIFF_TERM => "TRUE")

VHDL: port map (

VHDL: I => FOUT_P , IB => FOUT_N ,

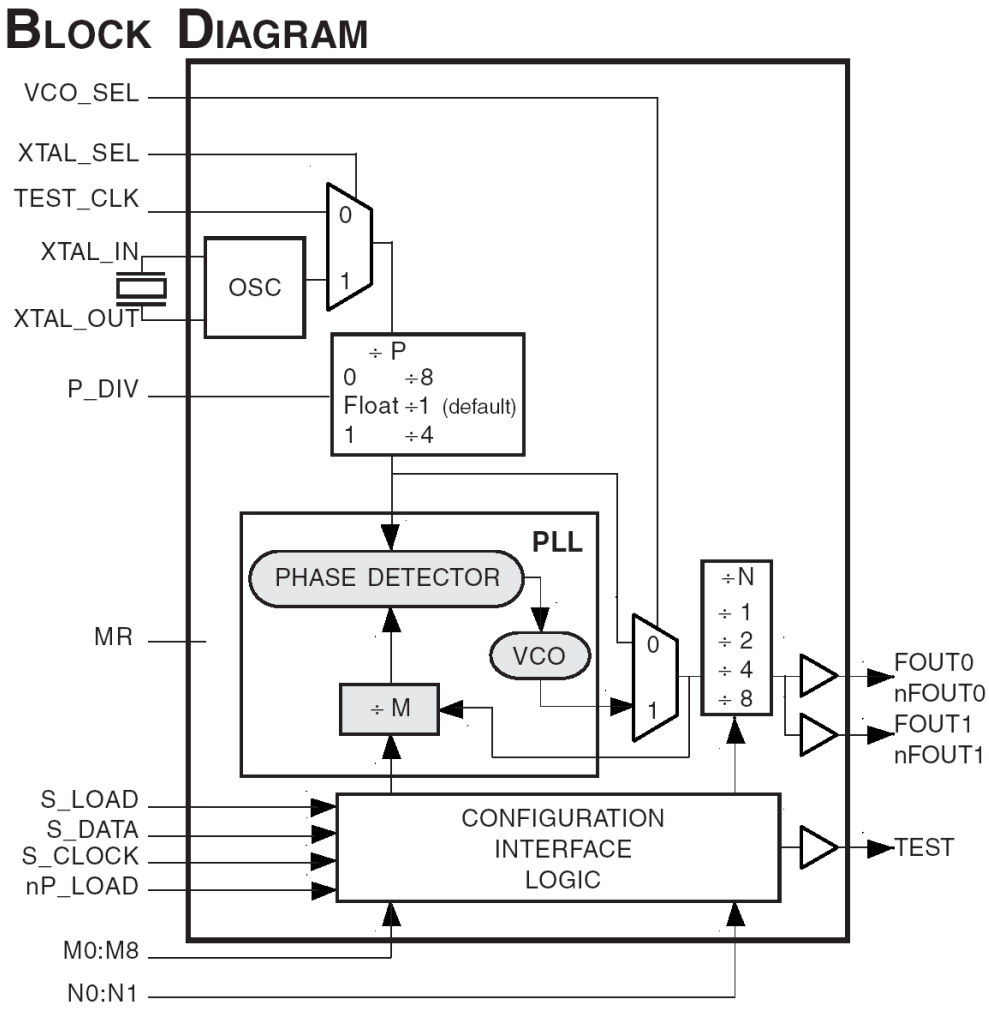
VHDL: O => FOUT_IGDS) ;

NOTE: By default the DDR PLL, U53, is in BYPASS MODE and only used as a voltage level shifter.

4.6 Configuring the ICS843020-01 [U44]

Note that the ICS843020-01 reference manual should be considered the authority concerning the ICS843020-01. The manual is available on the DNDVI CD as ICS843020-01.pdf and also from the ICS website.

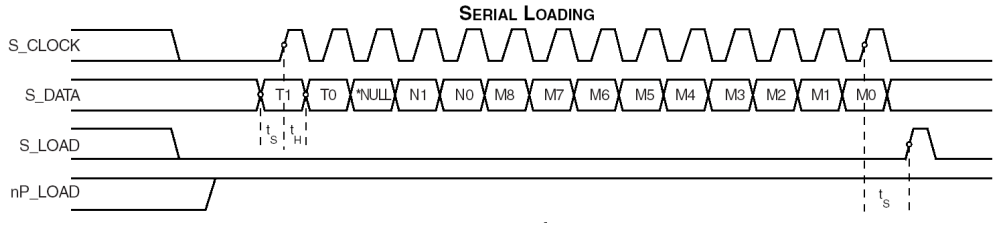
http://www.icst.com/datasheets/ics843020-01.pdf



The ICS843020-01 has two modes of operation: Input from TEST_CLK or input from XTAL_IN/OUT depending on the setting of XTAL_SEL. By default XTAL_SEL is set to 1 [XTAL_IN/OUT] to switch the input into the ICS843020-01 see the Schematic, one will need to move a configurable resistor going into XTAL_SEL.

The FOUT frequency is governed by **FOUT = F_IN * M/(2^N*P_DIV);** Where M is an integer and N is a power of two and P_DIV is 1, 4 or 8. FOUT is a LVDS differential signal and must be treated as such when being incorporated into the Verilog/VHDL design. Note that by default P_DIV is floating, to change the value of P_DIV see the schematic for which resistor to remove.

Only serial configuration is supported on the DN_DVI board which means the ICS843020-01 needs to be configured each time the board is reset.



In addition to the above discussed N and M inputs T configures the TEST output a pattern of {1,1} will set TEST to FOUT.

Note that the SDATA and SLOAD are the same for all the ICS8442s/ICS843020-01 on the DNDVI board and that each IC component can be programmed separately by control of the individual S_CLOCK signals. Please see the schematic for specific ICS843020-01s. The maximum frequency allowable for S_CLOCK is 50MHZ, LVCMOS.

When editing the constraints file for a design make sure the ICS843020-01 inputs are set to LVDSEXT_25; And that DIFF_TERM is used on the input buffer. [See note on Schematic P09_CLOCKS].

Example FOUT Verilog/VHDL/UCF settings:

UCF: NET "..FOUT.." LOC = … | IOSTANDARD = LVDSEXT_25;

Verilog: IBUFGDS

Verilog: #(.DIFF_TERM("TRUE"))

Verilog: IGDS_FOUT

Verilog: (.I(FOUT_P), .IB(FOUT_N), .O(FOUT_IGDS));

```
VHDL:       IGDS_FOUT: IBUFGDS
VHDL:           generic map (
VHDL:               DIFF_TERM => "TRUE" )
VHDL:           port map (
VHDL:               I => FOUT_P , IB => FOUT_N ,
VHDL:               O => FOUT_IGDS ) ;
```

Chapter

5

5 DVI Interfaces : Receivers and Transmitters

5.1 Receivers SiI163B

Note that the SiI 163B reference manual should be considered the authority concerning the SiI 163B. The manual is available on the DNDVI CD as SiI163b-DS-0055.pdf and also from the SiI website.

http://www.siimage.com/docs/SiI-DS-0055.pdf

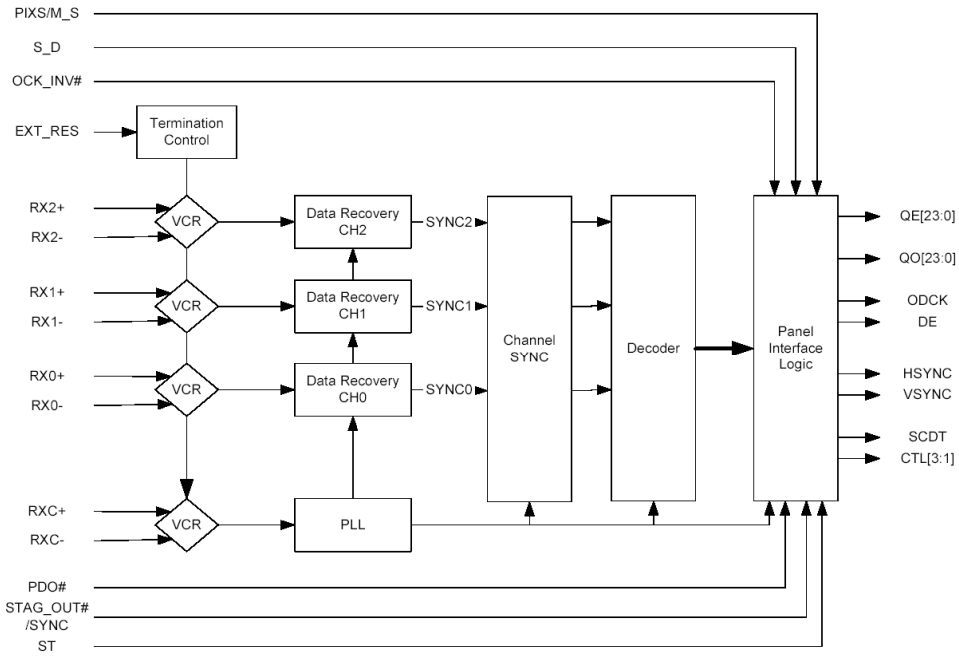


Figure 1. Functional Block Diagram

The DNDVI_DC board has two Sil 163B chips per receiver channel. One Sil 163B is designated as the MASTER and one as the SLAVE. When a single link signal is applied to the receiver the MASTER SiI 163B will handle all 48 bits of output. When a dual link signal is applied the Master SiI 163B will handle the even 24 bits and the Slave SiI163B will handle the odd 24 bits [**NOTE – The slave is bit-reversed!**]

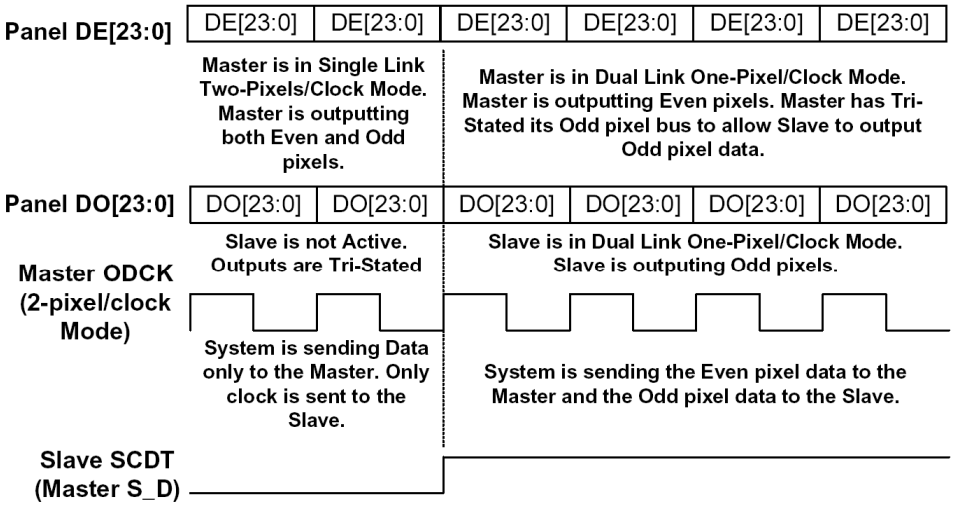
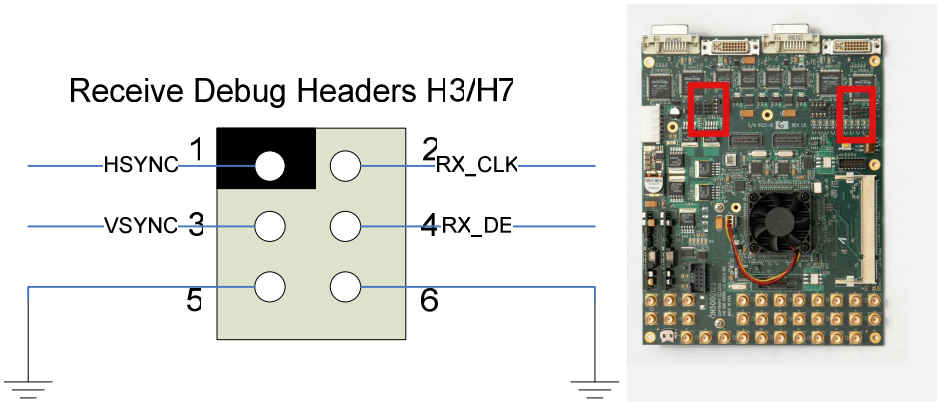
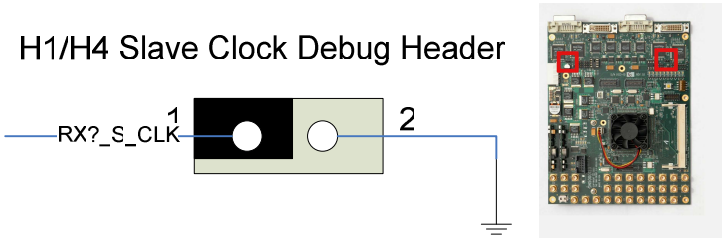

Panel DE[23:0]
DE[23:0]
DE[23:0]
DE[23:0]
DE[23:0]
DE[23:0]
DE[23:0]
Master is in Single Link Two-Pixels/Clock Mode. Master is outputting both Even and Odd pixels.
Master is in Dual Link One-Pixel/Clock Mode. Master is outputting Even pixels. Master has Tri-Stated its Odd pixel bus to allow Slave to output Odd pixel data.
Panel DO[23:0]
DO[23:0]
DO[23:0]
DO[23:0]
DO[23:0]
DO[23:0]
DO[23:0]
Slave is not Active. Outputs are Tri-Stated
Slave is in Dual Link One-Pixel/Clock Mode. Slave is outputing Odd pixels.
Master ODCK (2-pixel/clock Mode)
System is sending Data only to the Master. Only clock is sent to the Slave.
System is sending the Even pixel data to the Master and the Odd pixel data to the Slave.
Slave SCDT (Master S_D)

Figure 14. Single/Dual Link Timing Diagram

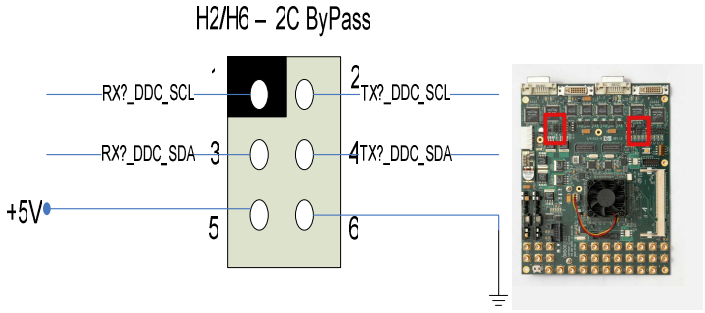
In the above diagram DE is RX?_QE_[23:0], DO is RX?_QO_[23:0]. [**NOTE – QO is bit-reversed in dual link mode!**]. Master ODCK is RX?_CLK.

HSYNC, VSYNC are also passed into the FPGA.





I2C Bypass: If so desired the I2C channel can be directly connected to the DVI transmitter. To do this one needs to remove the DDC EEPROM (U13/U20) [Default: Removed] and use jumpers to short the RX I2C to the TX I2C.



Please see the schematic for specific connection issues.

5.2 Transmitters SiI178

Note that the SiI 178 reference manual should be considered the authority concerning the SiI 178. The manual is available on the DNDVI CD as SiI178-DS-0086.pdf and also from the SiI website.

http://www.siliconimage.com/docs/SiI-DS-0086.pdf

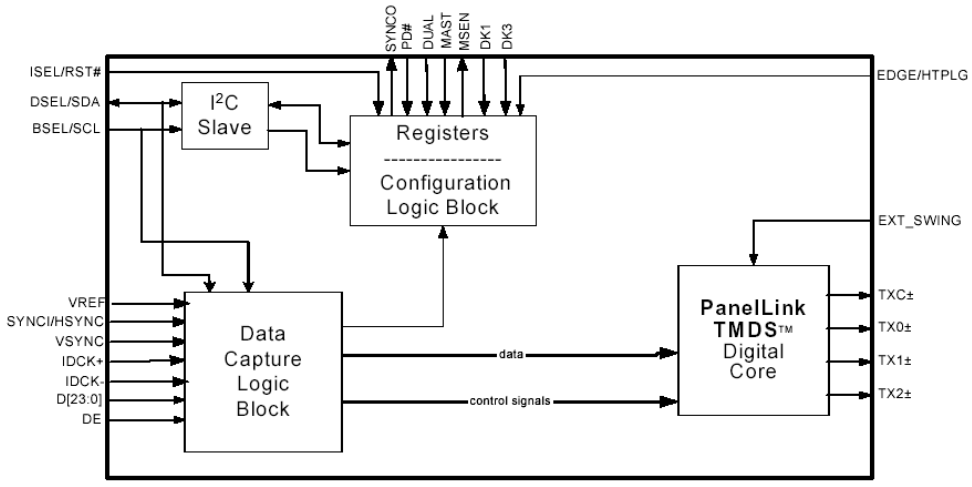


Figure 2. Functional Block Diagram

The DNDVI_DC board has two Sil 178 chips per transmitter channel. One Sil 178 is designated as the MASTER and one as the SLAVE. When a single link signal is applied to the transmitter the MASTER SiI 178 will handle all 24 bits of output. When a dual link signal is applied the Master SiI 178 will handle the lower 12 bits and the

Slave SiI178 will handle the upper 12 bits of each pixel. Note – while the SiI 178 is capable of both 24 bit and 12 bit input modes only the 12 bit input mode is available in dual link configurations.

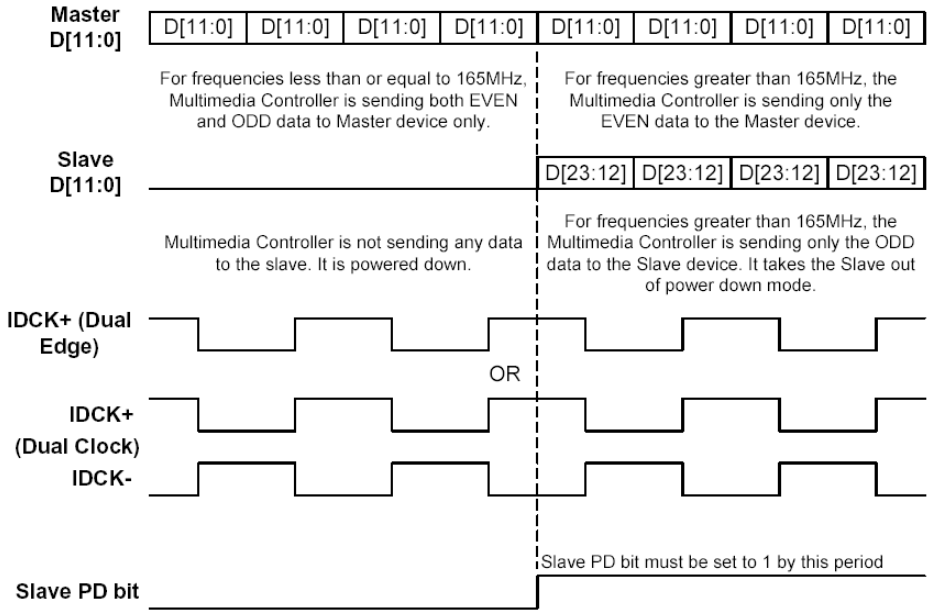

Master D[11:0]
D[11:0]
D[11:0]
D[11:0]
D[11:0]
D[11:0]
D[11:0]
D[11:0]
D[11:0]
For frequencies less than or equal to 165MHz, Multimedia Controller is sending both EVEN and ODD data to Master device only.
For frequencies greater than 165MHz, the Multimedia Controller is sending only the EVEN data to the Master device.
Slave D[11:0]
D[23:12]
D[23:12]
D[23:12]
D[23:12]
Multimedia Controller is not sending any data to the slave. It is powered down.
For frequencies greater than 165MHz, the Multimedia Controller is sending only the ODD data to the Slave device. It takes the Slave out of power down mode.
IDCK+ (Dual Edge)
OR
IDCK+ (Dual Clock)
IDCK-
Slave PD bit must be set to 1 by this period
Slave PD bit

Figure 15. Single/Dual Link Timing Diagram

The I2C address of the Master SiI178 is 0x70 and the address of the Slave SiI178 is 0x72 [Only after writing to 0x70 register PD set to 0 – this must be done after every reset, see SiI178 manual for explanation].

Chapter 6

6 Reference Design

This section will discuss the options available in the reference design along with the steps needed to generate bit files from the reference design using standard development tools.

The reference design provides an example interface to the RS232 port, DVI ports, and DDR2 module port. The provided design files can also be used to test the process of generating FPGA programming files and loading them into the FPGA.

6.1 Reference Design Verilog Files

Included on the CD are the Verilog files for the reference design. The top level file U1_fpga.v has several defines which determine the behavior of the design.

`define SETUP_8442

When defined the 8442s are configured.

`define EXPCONIO_TEST

When defined the 200 pin header is active and will respond to the daughter card header test. [This is used internally in the Dini group to verify functionality of the header. If one desires to use this test one will need a host card, such as the 8000k10pci, configured with the matching end of this test]

`define INCLUDE_DDR2_LOGIC

When defined the DDR2 test is enabled.

`define DDR2_LEDS

When defined the LEDS are used to indicate states of the DDR2 test.

`define DDR2_MICTOR_DEBUG

When defined the mictor connector will hold the data returned from a invalid ddr2 read if one exists. This is used internally.

`define RX0_PASSTHROUGH

When defined the RX0 DVI channel will be shunted to the TX0 DVI channel. When not defined TX0 will generate a basic test image.

`define RX1_PASSTHROUGH

When defined RX1 DVI channel will be shunted to the TX1 DVI channel. When not defined nothing happens to the transmitter.

`define TX0_PATTERN_2560x1600

`define TX0_PATTERN_1600x1200

`define TX0_PATTERN_1280x1024

`define TX0_PATTERN_640x480

Only one of the above should be defined at a time. When defined they specify the test pattern resolution displayed on TX0 if RX0_PASSTHROUGH is not defined.

`define H_MIRROR

This turns on the MIRROR output option for the RX_PASSTHROUGH defines above. The output will be the horizontal mirror of the input. See later parts of this section for demonstration. On S2 DIPSW4 is used to enable or disable output mirroring.

6.2 Synthesizing the Reference Design

Synthesis of the Dini Group reference design requires Synplicity's Synplify software. If you don't have this software you should get Synplicity's 30-day evaluation software. The reference design can be compiled using Xilinx's XST synthesis tool built in to ISE, but may need to be modified.

Using Simplify Pro open the dn123_synp.prj synplify file included on the CD. Make sure in the implementation options tab the correct Xilinx Part/Speed settings have been selected. Verify that the Verilog tab inside Implementation Options and change any Paths that have been defined to point to appropriate locations on the host system. Run Synplify.

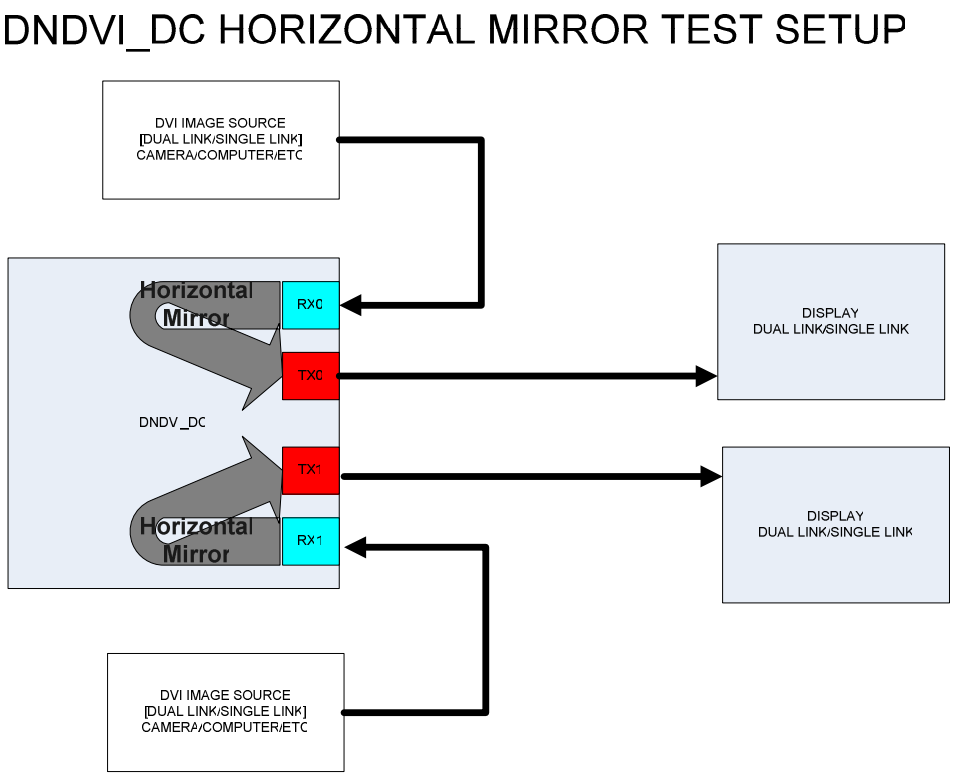
Create a new project in Xilinx ISE project navigator specify EDIF has the top level source. Select the Synplify output as the Input design. Make sure to deselect the "Copy the input design to the project directory" option. Select the U1_fpga.ucf file as the constraint file. Select the appropriate FPGA properties

on the next screen then finish creating the project. Right click on Translate and select properties – Make sure the Allow Unmatched LOC Constraints option is enabled. Generate the programming file by double clicking on Generate Programming File.

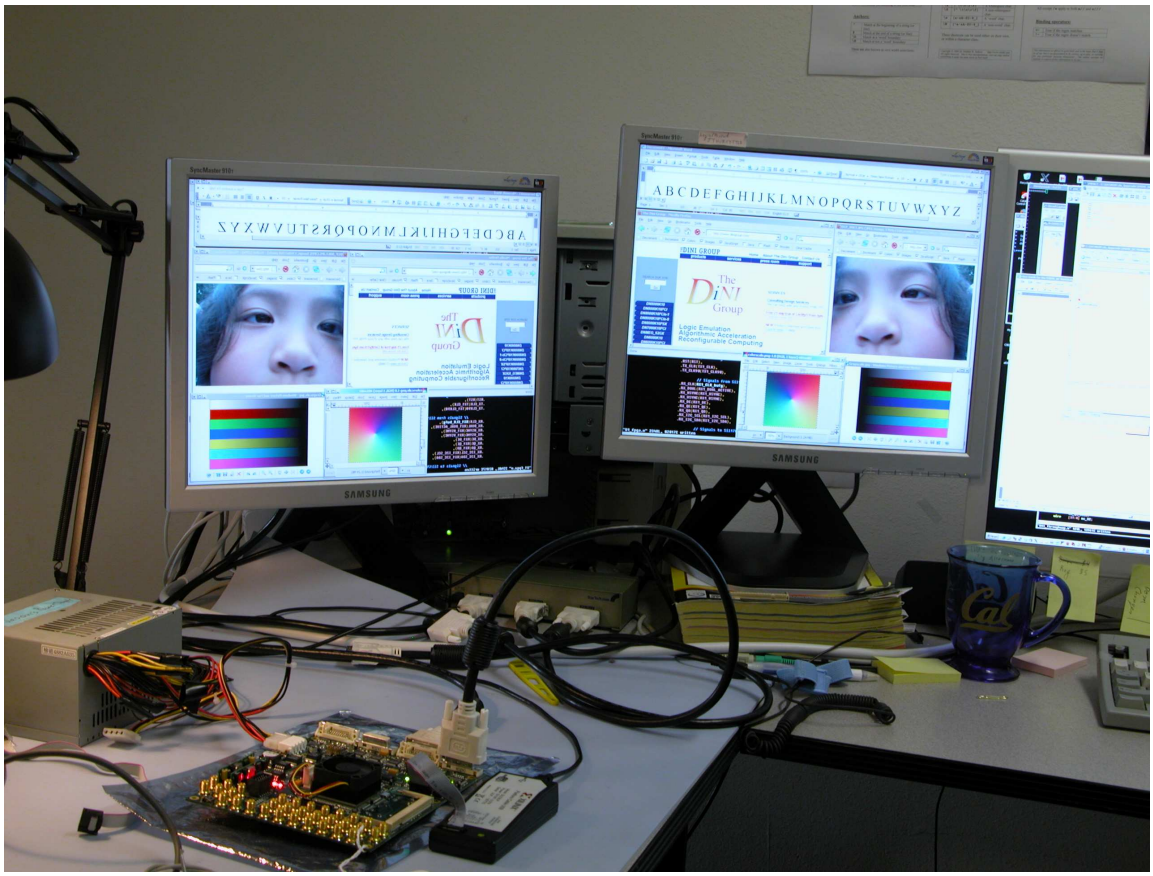
At this point a bit file should be created, load it into the DNDVI_DC board following the steps outlined in section 1.4.

6.3 Horizontal Mirroring

After recompiling the bitfile including the H_MIRROR option the following demonstration can be performed.



With the following results:



Note that dip switch S2 leaver 4 can be used in this mode to switch between mirrored output and non-mirrored output.

Also note that a different bitfile will be needed for single link and dual link applications.

Important: If for some reason noise exists on the screen or the clock is dysynched press the RESET button (S1).